AMENDMENT TO THE CLAIMS

1-3. (Canceled)

4. (Original) A semiconductor integrated circuit device comprising:

a first circuit pattern having a first linear pattern and placed in a region in which a group of elements having a repetitive pattern are formed; and

a second circuit pattern having a second linear pattern and placed in a region in which components other than the group of elements are formed,

a dummy pattern being inserted in the region in which the second circuit pattern is placed such that a sum perimeter of the first linear pattern, the second linear pattern, and the dummy pattern per unit area is equal to or less than a perimeter of the first linear pattern per unit area.

5. (Original) The semiconductor integrated circuit device of claim 4, wherein the group of elements are memories.

6. (Original) The semiconductor integrated circuit device of claim 4, wherein a perimeter of the dummy pattern per unit area is 70% or more of the perimeter of the first linear pattern per unit area.

7-16. (Canceled)

17. (New) A semiconductor integrated circuit device comprising:

a first circuit pattern having a first gate electrode pattern and placed in a memory circuit region; and

a second circuit pattern having a second gate electrode pattern and placed in a logic circuit region,

a dummy pattern being inserted in the logic region in which the second circuit pattern is placed such that a sum perimeter of the first gate electrode pattern, the second gate electrode pattern, and the dummy pattern per unit area is equal to or less than a perimeter of the first gate electrode pattern per unit area.

18. (New) The semiconductor integrated circuit device of claim 17, wherein the dummy pattern has a rectangular like shape.

19. (New) The semiconductor integrated circuit device of claim 17, wherein the perimeter of the dummy pattern per unit area is 70% or more of the perimeter of the first gate electrode pattern per unit area.